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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,790	HONARY ET AL.	
	Examiner	Art Unit	
	AIMEE J. LI	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,8-10,13,16,17 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,8-10,13,16,17 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/29/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 2, 5, 8-10, 13, 16, 17, and 20-22 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as filed 29 September 2008 and Amendment as filed 03 December 2008.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 29 September 2008 was filed after the mailing date of the Non-Final Rejection on 03 September 2008. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 5, 8, 9, 10, 13, 16, 17, 20, 21, and 22 are rejected under 35 U.S.C. 102(b) as being taught by Gove et al., U.S. Patent Number 5,212,777 (herein referred to as Gove).

6. Referring to claim 1, Gove has taught an apparatus, comprising:

a. A memory unit to store data (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);

b. A plurality of parallel data paths to process said data (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);

c. A plurality of control units to control said data paths (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62); and

d. A switch to connect said control units to said data paths, said switch to receive configuration information to establish a first set of connections between at least one of said control units and multiple data paths to execute a first process using single instruction multiple data processing with said at least one control unit to control said multiple data paths, and a second set of connections between multiple control units and multiple data paths to execute a second process using multiple instruction multiple data processing with each control unit to control a single data path (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 25, lines 44-54; column 61, line 60 to column 62, line 24; column 62, lines 40-52; column 63, lines 4-20; column 170, lines 50-62; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; Figure 62; and Figure 64 – In regards to Gove, the SIMD/MIMD Hybrid

shown in Figure 64 shows that SIMD and MIMD processes performed in parallel with some of the data paths and controllers configured for SIMD operation and some are configured for MIMD operation.);

e. Wherein said data paths are configured based upon said connections between said control units and said data paths to perform said first process and said second process in parallel (Gove column 25, lines 44-54; column 62, lines 40-52; column 63, lines 4-20; column 170, lines 50-62; and Figure 64 – In regards to Gove, the SIMD/MIMD Hybrid shown in Figure 64 shows that SIMD and MIMD processes performed in parallel with some of the data paths and controllers configured for SIMD operation and some are configured for MIMD operation.),

f. The configuration information received on each clock cycle from one or more of the control units (Gove column 2, lines 13-17; column 3, lines 5-20; and column 5, lines 20-34; and Figure 1 - In regards to Gove, the SIMD/MIMD modes are switched on a cycle by cycle basis, which means that the configuration information designating which mode the processor is operating in.).

7. Referring to claim 2, Gove has taught the apparatus of claim 1, wherein each control unit controls execution of a single program instruction (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

8. Referring to claim 5, Gove has taught the apparatus of claim 1, wherein each data path performs a same set of operations using said data (Gove column 1, line 47 to column 3, line 20;

column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

9. Referring to claim 8, Gove has taught the apparatus of claim 1, wherein each data path performs a different set of operations using said data (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

10. Referring to claim 9, Gove has taught the apparatus of claim 1, further comprising a configuration module to configure said switch to establish said connections in accordance with said configuration information (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

11. Referring to claim 10, Gove has taught a system, comprising:

g. An antenna (Gove column 5, lines 49-56; column 28, lines 63-64; column 66, lines 3-8; and Figure 48). In regards to Gove, antennas send and receive signals for devices, such as televisions and remote cameras (Please see www.dictionary.com "antenna" ©2000).

h. A host processing system (Gove column 2, line 66 to column 3, line 4; column 5, lines 20-34; column 6, lines 23-36; column 12, line 63 to column 13, line 9; Figure 1l Figure 2; Figure 4; Figure 17; and Figure 29);

i. A configuration module to store configuration information (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62); and

j. A reconfigurable communication architecture module to receive said configuration information (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62) comprising:

i. A plurality of processing elements to execute functions for each process (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62), said plurality of processing elements comprising

(1) A memory unit to store data (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);

(2) A plurality of parallel data paths to process said data (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);

(3) A plurality of control units to control said data paths (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62); and

(4) A switch to connect said control units to said data paths, said switch to receive said configuration information to establish a first set of connections between at least one of said plurality of control units and multiple data paths to execute said first process, and a second set of connections between multiple control units and multiple data paths to execute said second process (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 25, lines 44-54; column 61, line 60 to column 62, line 24; column 62, lines 40-52; column 63, lines 4-20; column 170, lines 50-62; Figure 1; Figure 2; Figure

4; Figure 14; Figure 15; Figure 17; Figure 61; Figure 62; and Figure 64 – In regards to Gove, the SIMD/MIMD Hybrid shown in Figure 64 shows that SIMD and MIMD processes performed in parallel with some of the data paths and controllers configured for SIMD operation and some are configured for MIMD operation.)

ii. A plurality of routing elements to connect said processing elements (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62); and

iii. A plurality of communications mediums to connect said processing elements and said routing elements in a mesh topology (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62). In regards to Gove, a "mesh topology" is where multiple nodes are connected together with multiple connections (Please see www.its.bldrdoc.gov "mesh topology" ©1996), which is shown in Gove's Figures 4 and 17.

k. Said reconfigurable communication architecture module to configure itself to perform single instruction multiple data processing in said first configuration to execute said first process, and to perform multiple instruction multiple data processing in said

second configuration to execute said second process (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);

l. Wherein said routing elements are configured based upon said connections between said processing elements and said routing elements to perform said first process and said second process in parallel (Gove column 25, lines 44-54; column 62, lines 40-52; column 63, lines 4-20; column 170, lines 50-62; and Figure 64 – In regards to Gove, the SIMD/MIMD Hybrid shown in Figure 64 shows that SIMD and MIMD processes performed in parallel with some of the data paths and controllers configured for SIMD operation and some are configured for MIMD operation.),

m. The configuration information received on each clock cycle from one or more of the plurality of processing elements (Gove column 2, lines 13-17; column 3, lines 5-20; and column 5, lines 20-34; and Figure 1 - In regards to Gove, the SIMD/MIMD modes are switched on a cycle by cycle basis, which means that the configuration information designating which mode the processor is operating in.).

12. Referring to claim 13, Gove has taught the system of claim 10, wherein each control unit controls execution of a single program instruction (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

13. Referring to claim 16, Gove has taught a method, comprising:

n. Receiving configuration information at a switch (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62); and

o. Configuring said switch to establish a first set of connections between at least on of a plurality of control units and multiple data paths to execute a first process using single instruction multiple data processing with said at least one control unit to control said multiple data paths(Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62); and

p. Configuring said switch to establish a second set of connections between multiple control units and multiple data paths to execute a second process using multiple instruction multiple data processing with each control unit to control a single data path (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);

q. Wherein said data paths are configured based upon said connections between said control units and said data paths to perform said first process and said second process in

parallel (Gove column 25, lines 44-54; column 62, lines 40-52; column 63, lines 4-20; column 170, lines 50-62; and Figure 64 – In regards to Gove, the SIMD/MIMD Hybrid shown in Figure 64 shows that SIMD and MIMD processes performed in parallel with some of the data paths and controllers configured for SIMD operation and some are configured for MIMD operation.),

r. The configuration information received on each clock cycle from one or more of the control units (Gove column 2, lines 13-17; column 3, lines 5-20; and column 5, lines 20-34; and Figure 1 - In regards to Gove, the SIMD/MIMD modes are switched on a cycle by cycle basis, which means that the configuration information designating which mode the processor is operating in.).

14. Referring to claim 17, Gove has taught the method of claim 16, wherein each control unit controls execution of a single program instruction (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

15. Referring to claim 20, Gove has taught the method of claim 16, further comprising:

s. Receiving a first set of data (Gove column 8, line 42 to column 9, line 13; column 10, lines 5-8, 22-29, and 38-44; column 10, line 65 to column 11, line 30; column 61, line 60 to column 62, line 24; Figure 12; Figure 13; Figure 14; Figure 15; Figure 61; and Figure 62)

t. Storing said first set of data in a memory unit (Gove column 8, line 42 to column 9, line 13; column 10, lines 5-8, 22-29, and 38-44; column 10, line 65 to column 11, line

30; column 61, line 60 to column 62, line 24; Figure 12; Figure 13; Figure 14; Figure 15; Figure 61; and Figure 62); and

u. Processing said first set of data with said data paths using said first set of connections (Gove column 8, line 42 to column 9, line 13; column 10, lines 5-8, 22-29, and 38-44; column 10, line 65 to column 11, line 30; column 61, line 60 to column 62, line 24; Figure 12; Figure 13; Figure 14; Figure 15; Figure 61; and Figure 62).

16. Referring to claim 21, Gove has taught the method of claim 16, further comprising:

v. Receiving a second set of data (Gove column 8, line 42 to column 9, line 13; column 10, lines 5-8, 22-29, and 38-44; column 10, line 65 to column 11, line 30; column 61, line 60 to column 62, line 24; Figure 12; Figure 13; Figure 14; Figure 15; Figure 61; and Figure 62);

w. Storing said second set of data in a memory unit (Gove column 8, line 42 to column 9, line 13; column 10, lines 5-8, 22-29, and 38-44; column 10, line 65 to column 11, line 30; column 61, line 60 to column 62, line 24; Figure 12; Figure 13; Figure 14; Figure 15; Figure 61; and Figure 62); and

x. Processing said second set of data with said data paths using said second set of connections (Gove column 8, line 42 to column 9, line 13; column 10, lines 5-8, 22-29, and 38-44; column 10, line 65 to column 11, line 30; column 61, line 60 to column 62, line 24; Figure 12; Figure 13; Figure 14; Figure 15; Figure 61; and Figure 62).

17. Referring to claim 22, Gove has taught an article comprising:

y. A storage medium (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13;

column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);

z. Said storage medium including stored instructions that, when executed by a processor, result in receiving configuration information at a switch, configuring said switch to establish a first set of connections between at least one of a plurality of control units and multiple data paths to execute a first process using single instruction multiple data processing with said at least one control unit to control said multiple data paths, and configuring said switch to establish a second set of connections between multiple control units and multiple data paths to execute a second process using multiple instruction multiple data processing with each control unit to control a single data path (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);

aa. Wherein said data paths are configured based upon said connections between said control units and said data paths to perform said first process and said second process in parallel (Gove column 26, lines 44-54; column 62, lines 40-52; column 63, lines 4-20; column 170, lines 50-62; and Figure 64 – In regards to Gove, the SIMD/MIMD Hybrid shown in Figure 64 shows that SIMD and MIMD processes performed in parallel with some of the data paths and controllers configured for SIMD operation and some are configured for MIMD operation.),

18. The configuration information received on each clock cycle from one or more of the control units (Gove column 2, lines 13-17; column 3, lines 5-20; and column 5, lines 20-34; and Figure 1 - In regards to Gove, the SIMD/MIMD modes are switched on a cycle by cycle basis, which means that the configuration information designating which mode the processor is operating in.).

Response to Arguments

19. Applicant's arguments filed 03 December 2008 have been fully considered but they are not persuasive. Applicants' argue in essence on pages 7-10

> …the claimed subject matter teaches performing a first process (e.g. SIMD) and a second process (MIMD) in parallel with configuration information received on each clock cycle from one or more of the control units. Applicant respectfully submits that he has been unable to locate any teaching in Gove directed to the above recited language…

20. This has not been found persuasive.

21. As the Examiner pointed out in the Non-Final rejection mailed 03 September 2008, Gove teaches in column 2, lines 13-17; column 3, lines 5-20; and column 5, lines 20-34; and Figure 1 that the SIMD/MIMD modes are switched on a cycle by cycle basis, which means that the configuration information designating which mode the processor is operating in.

22. As pointed out in the Final rejection mailed 07 April 2008, Gove has taught a SIMD/MIMD hybrid functionality is possible with in his processor system. Gove explicitly states in column 26, lines 44-54 "…Register 2820 contains the current operating mode of the system. This register contains bits which indicate whether the system is MIMD, SIMD, or some

combination (hybrid) of SIMD and MIMD." Gove also explicitly states in column 62, lines 40-52 "…In this example, processors 100 and 101 have been configured in SIMD operation by sharing a common instruction memory and by utilizing the synchronization signals of bus 40. Processors 102 and 104 are utilizing separate instruction memories and are ignoring the synchronization signals of bus 40 and are thus running in MIMD mode." As shown in Figure 64, the SIMD/MIMD hybrid has some data paths working in SIMD mode while the other data paths work in MIMD mode. The data paths working in SIMD mode have all the data paths and associated control units connected together to the same instruction memory and receive the controlling synchronization signals, while, in MIMD mode, the data paths and associated control units are connected so separate, individual instruction memories and ignore the synchronization signals. Thus, Gove teaches that when SIMD and MIMD mode are operated in parallel, there is a first set of connections established between the multiple data paths and their respective control units to a single controlling instruction memory and synchronization signals and a second set of connections established between the multiple data paths and respective control units to separate controlling instruction memories.

23. Therefore, Gove teaches that the mode can be changed on a cycle by cycle basis and that his system can operate in SIMD and MIMD in parallel.

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

25. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AIMEE J. LI whose telephone number is (571)272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aimee J Li/
Primary Examiner, Art Unit 2183
15 March 2009